ABSTRACT OF THE DISCLOSURE

[0026] Testing of on-chip test structures is accomplished by employing a test apparatus that allows test data to be uploaded into selected data latches associated with respective ones of a plurality of test structures. Tests are performed by selectively providing a test data from the data latch to the associated test structure. Test results may be registered into an adjacent data latch for downloading. Multiple test structures may thereby be tested using only limited probing pad access and wafer area.